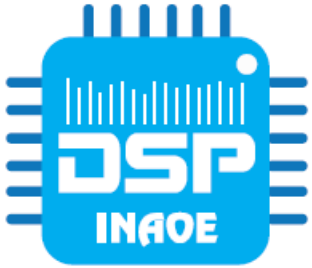
TWO-STAGE COMB DECIMATOR WITH IMPROVED FREQUENCY CHARACTERISTIC

Gerardo Molina Salgado[1],
Gordana Jovanovic Dolecek[1],
José de la Rosa[2],

Institute INAOE[1] and IMSE-CNM[2]



This paper presents comb-based decimation structures for high values of decimation factors in which the decimation factor can be presented as a power of *x*, where *x* is a prime number. Additionally, it presents slight modifications of the proposed structures, which do not affect the power and area efficiency, but improve the frequency response.

OUTLINE

1. INTRODUCTION
2. POWER AND AREA ESTIMATION
3. PROPOSED STRUCTURES
4. ALIAS REJECTION IMPROVEMENT
5. VHDL IMPLEMENTATION
6. CONCLUSION

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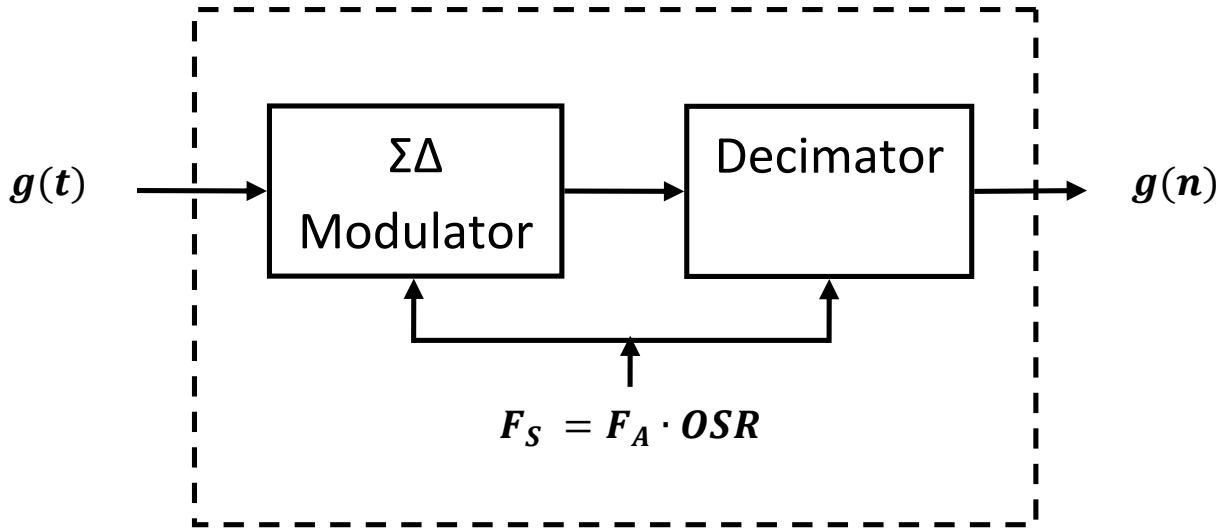
Sigma-Delta Analog-to-Digital Converter (ΣΔ-ADC)



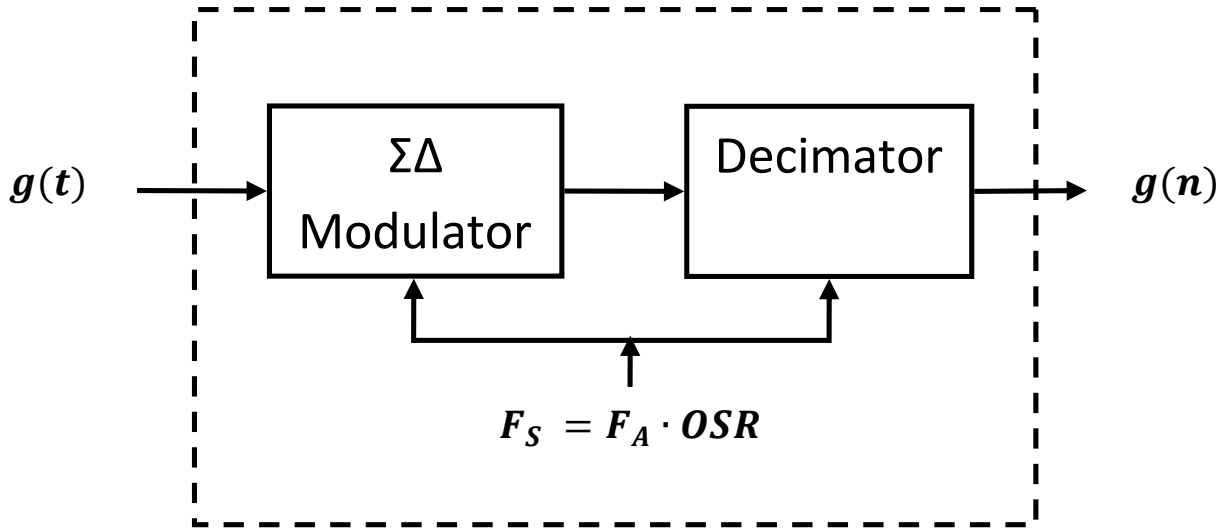
ΣΔM features:

- Analog signal is oversampled
- Quantization Noise is shaped

Decimator features:

- Remove out-of-band noise
- Decreases the sampling frequency

Sigma-Delta Analog-to-Digital Converter (ΣΔ-ADC)

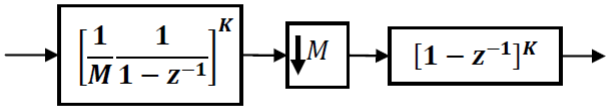


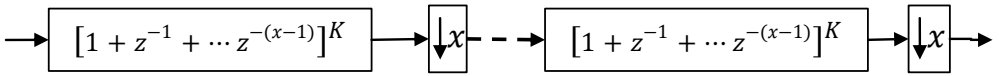
- The ΣΔ modulator is the most limiting circuit.
- However, the decimator must be optimized in terms of power, silicon area and frequency response.

Decimator comb structures

Recursive (CIC)

Non-Recursive ($M=x^P$)





Stage 1 Stage $\text{Log}_x(M)$

Small area.

Large power.

Opposite

each other

Low power.

Large area.

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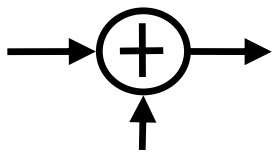
Power estimation in comb-based decimation filters

$$P = \gamma \cdot (FA + FF) B_{out}$$

ADDER



FA=Number of Full-Adders

FLIP-FLOP

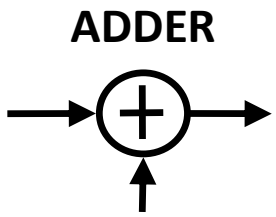
FF=Number of Flip-Flops

γ=relative sampling frequency

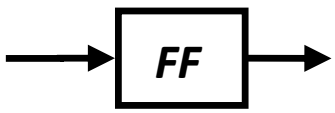
$$B_{out} = B_{in} + K \cdot log_2(M)$$

Area estimation in comb-based decimation filters

$$A = (FA + FF)B_{out}$$



FA=Number of Full-Adders

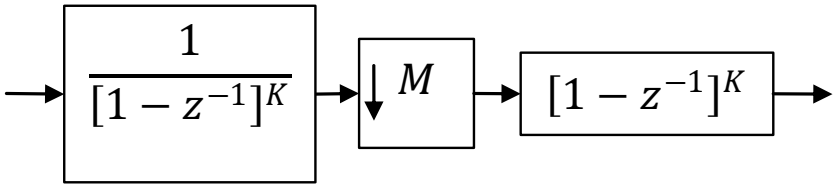


FF=Number of Flip-Flops

$$B_{out} = B_{in} + K \cdot log_2(M)$$

The sampling frequency has no impact on area estimation!

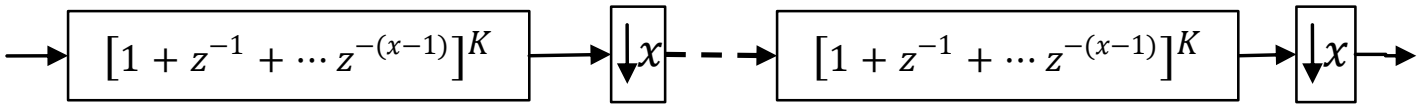
Power and area estimation for CIC



$$P_{CIC} = (FA_I + FF_I)B_{out} + \frac{(FA_C + FF_C)B_{out}}{x^P}$$

$$A_{CIC} = [(FA_I + FF_I) + (FA_C + FF_C)]B_{out}$$

Power and area estimation for NR-comb (Non-recursive) with $M=x^P$



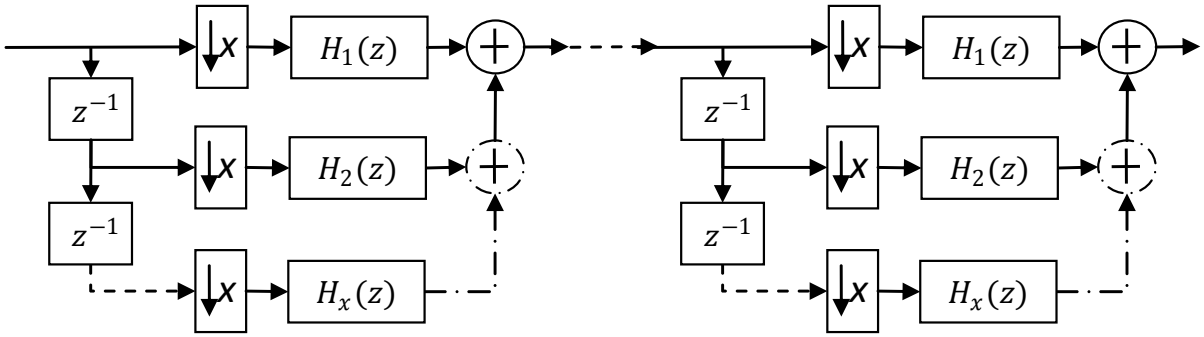
Stage 1 Stage $\text{Log}_x(M)$

$$P_{NRC-x} = \sum_{i=1}^{P} \frac{(FA_{NCS} + FF_{NCS}) \cdot \lceil B_{in} + K \cdot log_2(x^i) \rceil}{x^{i-1}}$$

$$A_{NRC-x} = \sum_{i=1}^{P} (FA_{NCS} + FF_{NCS}) \cdot \lceil B_{in} + K \cdot log_2(x^i) \rceil$$

x is a prime number

Power and area estimation for polyphase comb with $M=x^P$



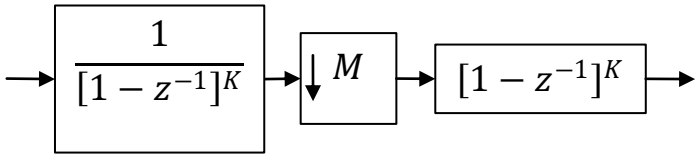
$$P_{PC-x} = \sum_{i=1}^{P} \frac{(FA_{PCS} + FF_{PCS}) \cdot \lceil B_{in} + K \cdot log_2(x^i) \rceil}{x^i}$$

$$A_{PC-x} = \sum_{i=1}^{P} (FA_{PCS} + FF_{PCS}) \cdot \lceil B_{in} + K \cdot log_2(x^i) \rceil$$

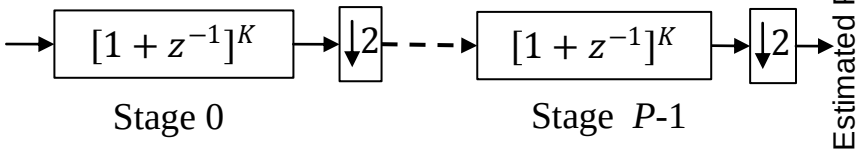
x is a prime number

Estimated power for CIC, NR-Comb and polyphase comb for $M=2^P$

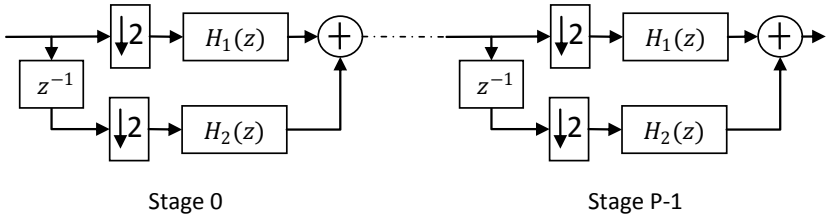
CIC

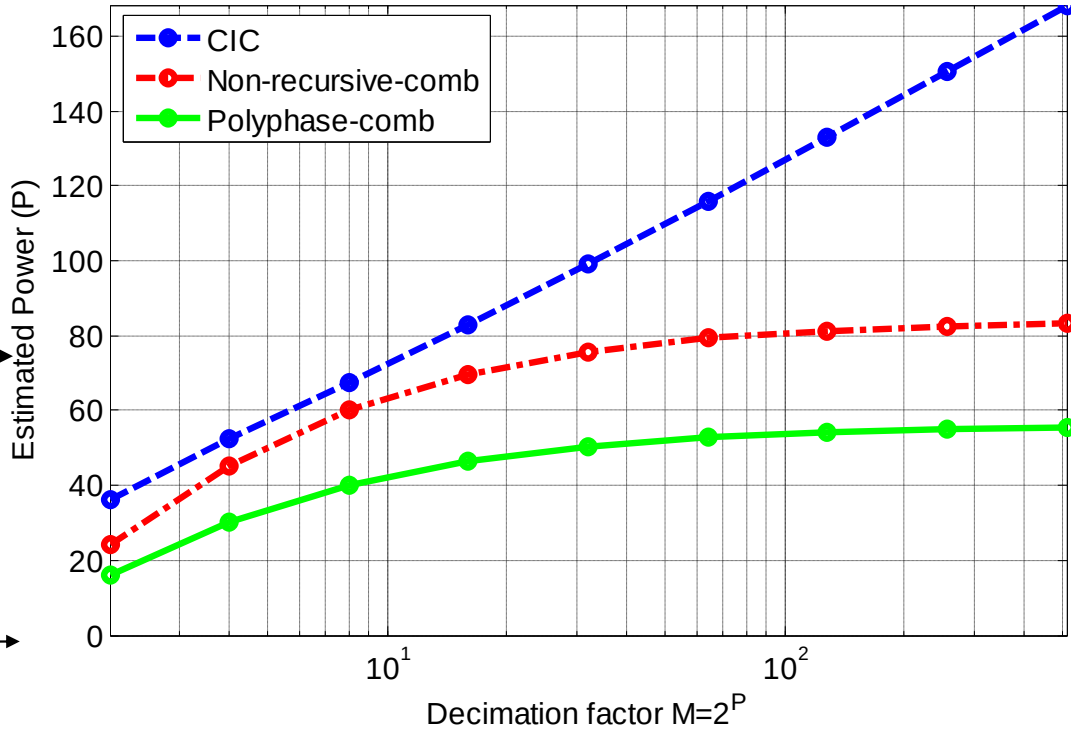


Non-recursive comb



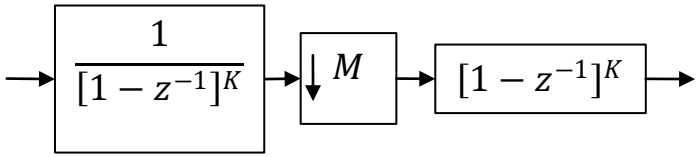
Polyphase comb



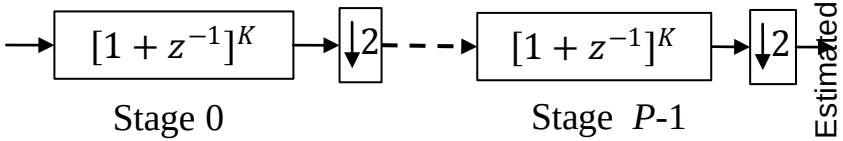


Estimated area for CIC, NR-Comb and polyphase comb for $M=2^P$

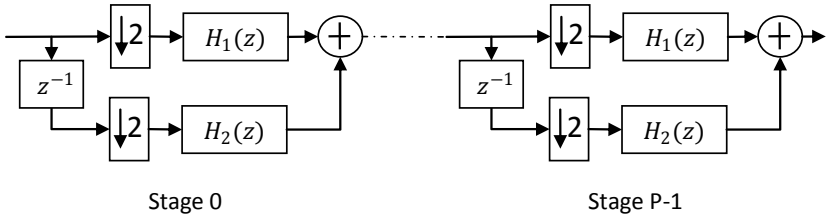
CIC

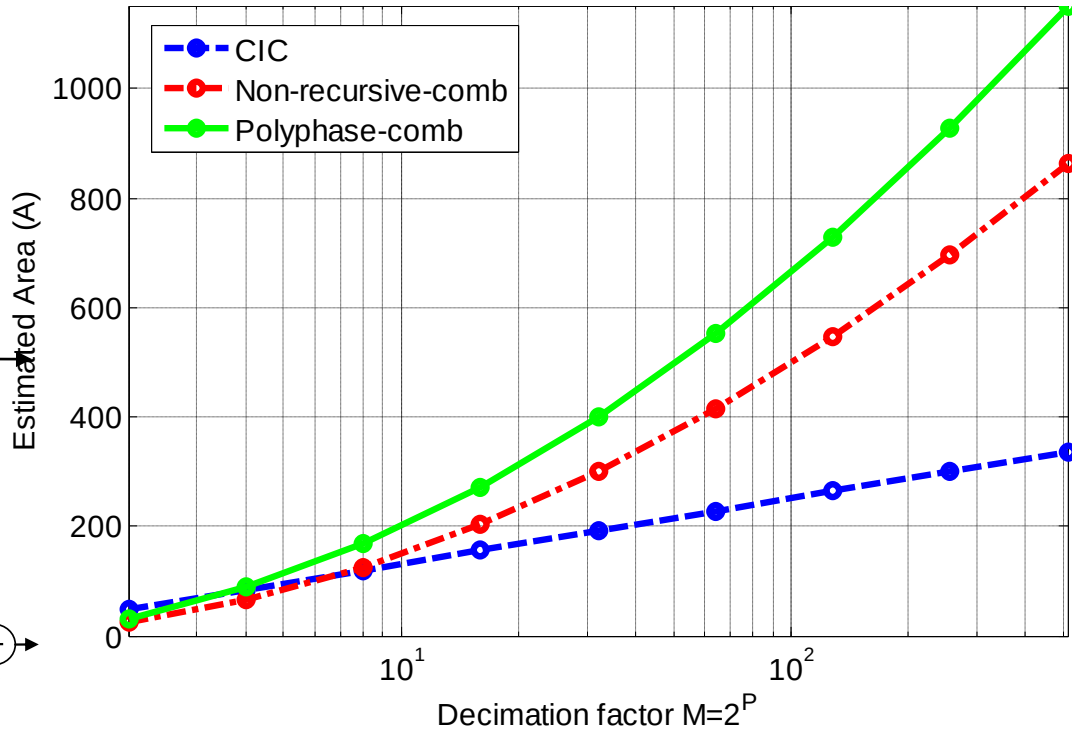


Non-recursive comb



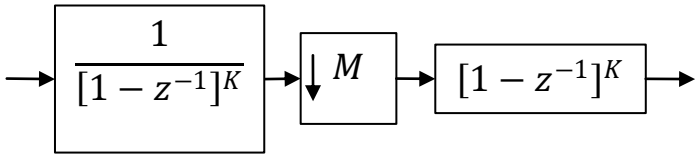
Polyphase comb



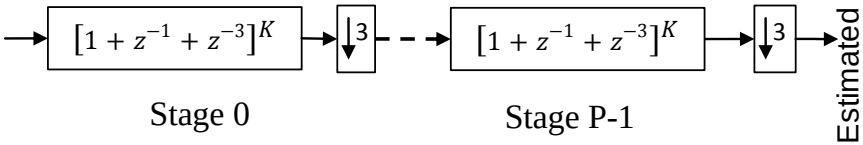


Estimated power for CIC, NR-Comb and polyphase comb for $M=3^P$

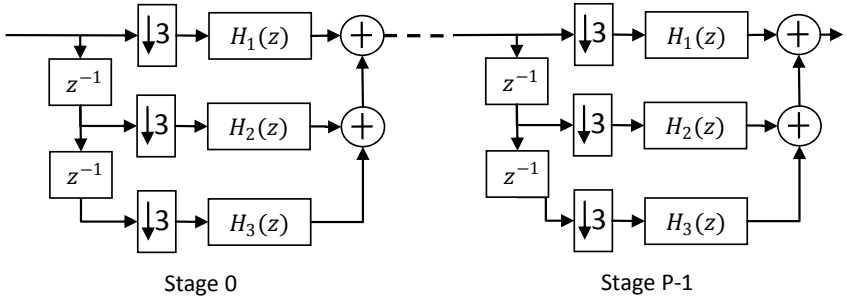
CIC

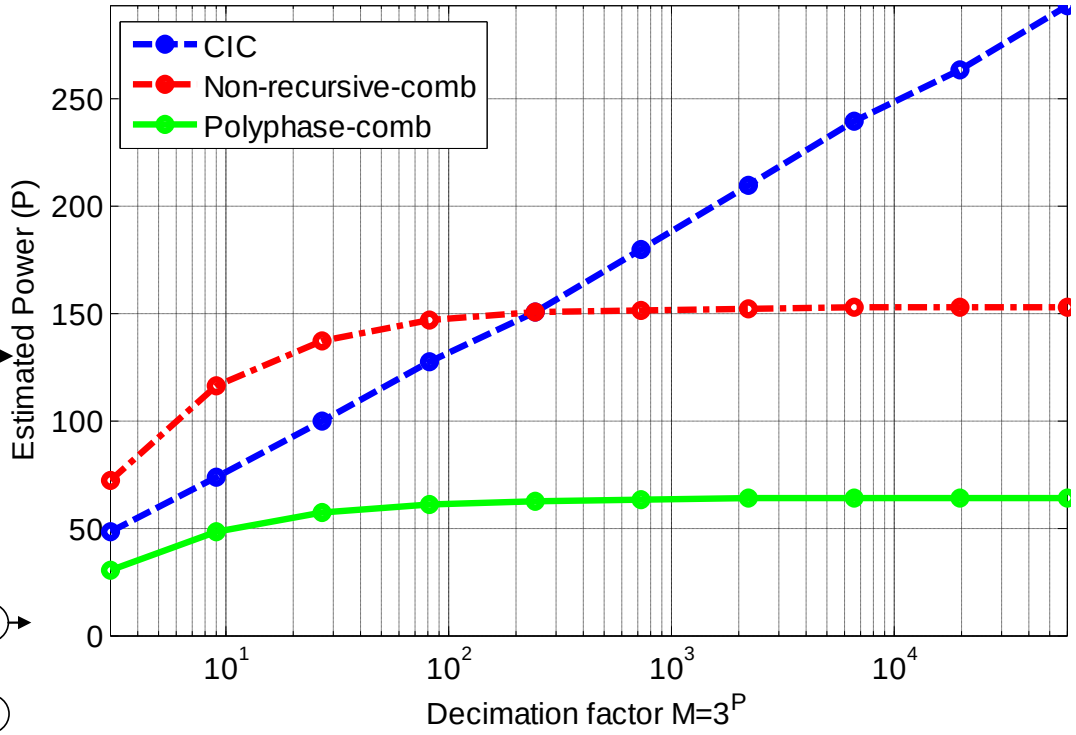


Non-recursive comb



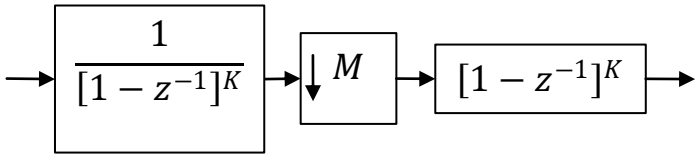
Polyphase comb



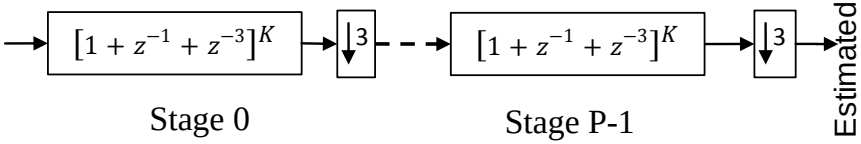


Estimated area for CIC, NR-Comb and polyphase comb for $M=3^P$

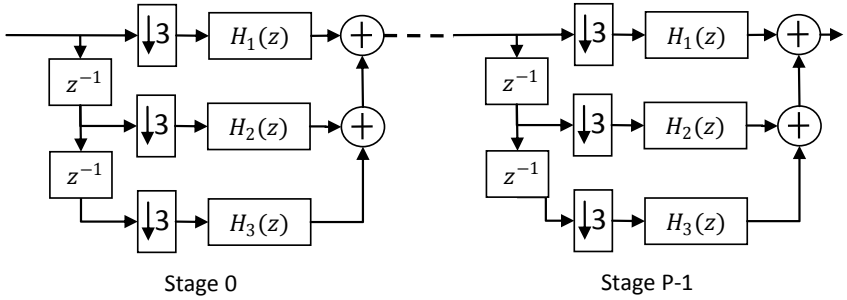
CIC

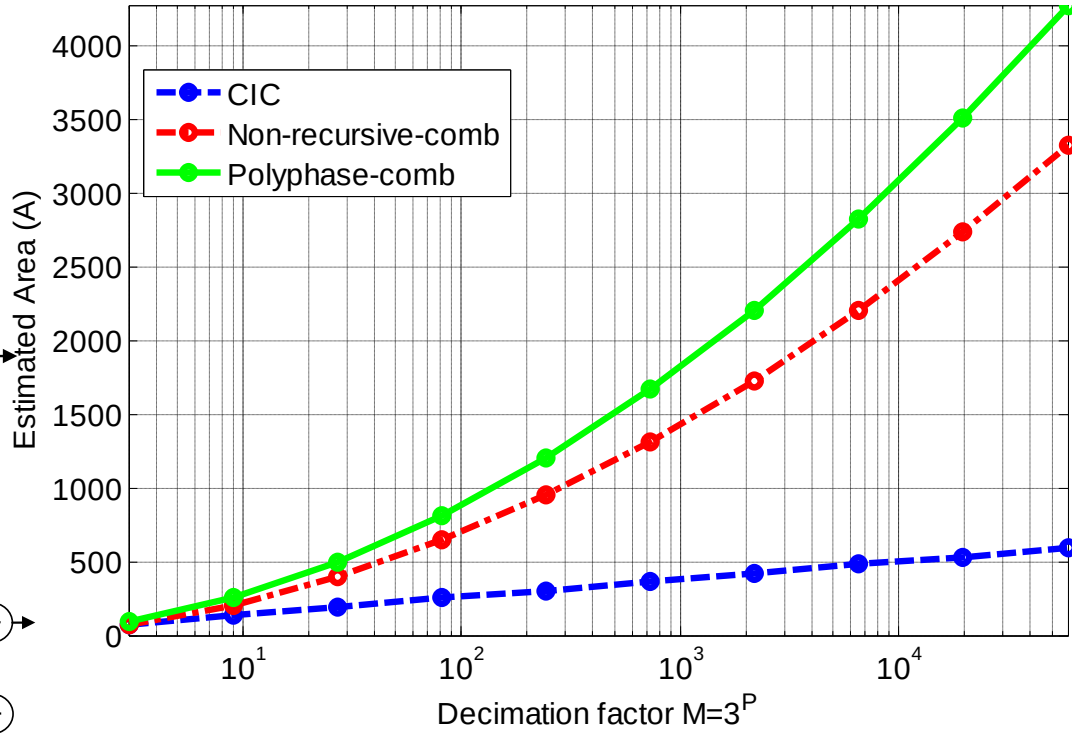


Non-recursive comb



Polyphase comb

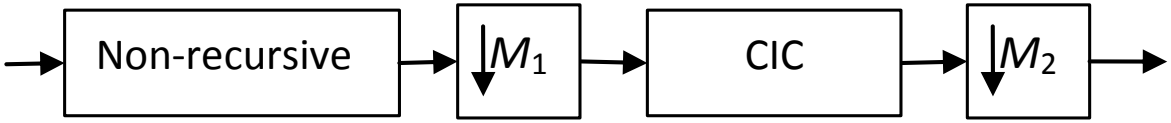




OUTLINE

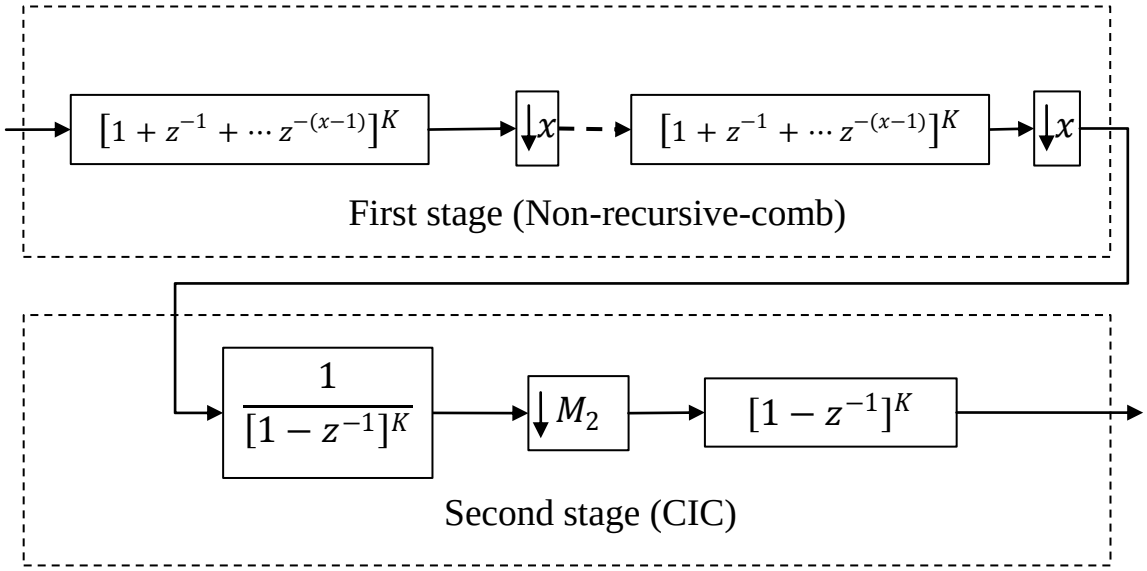
1. INTRODUCTION
2. TWO-STAGE STRUCTURE WITH CORRECTOR FILTER
3. PROPOSED STRUCTURE
4. COMPARISON WITH OTHER METHODS
5. VHDL-FPGA IMPLEMENTATION
6. CONCLUSION

Two-stage structure



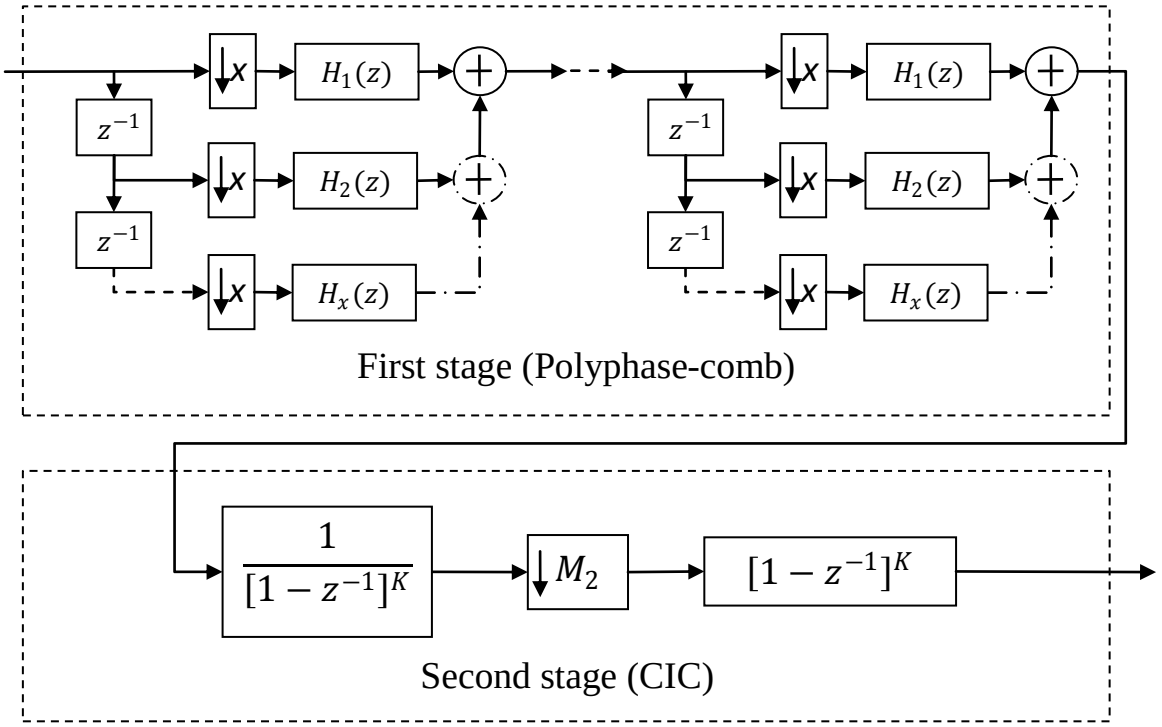
$$M=M_1M_2=x^P$$

NR-Comb-1



$$M=M_1M_2=x^P$$

NR-Comb-2



$$M=M_1M_2=x^P$$

There are P-1 different combinations for M_1 and M_2

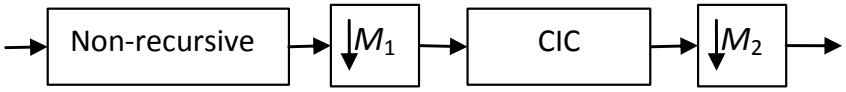
How to chose M_1 and M_2?

Chose M_1 in such a way that the estimated power of the Two-Stage structure is as close as possible to the non-recursive comb, but at the same time the area should be as close as possible to that used by a CIC structure.

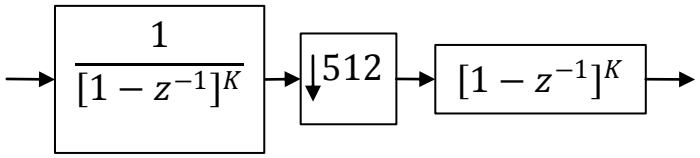
The *NR-CIC-1* structure for $M=2^P$

Example for M=512 (power estimation)

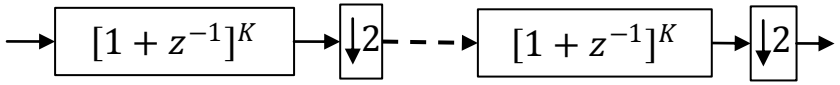
NR-CIC-1 structure



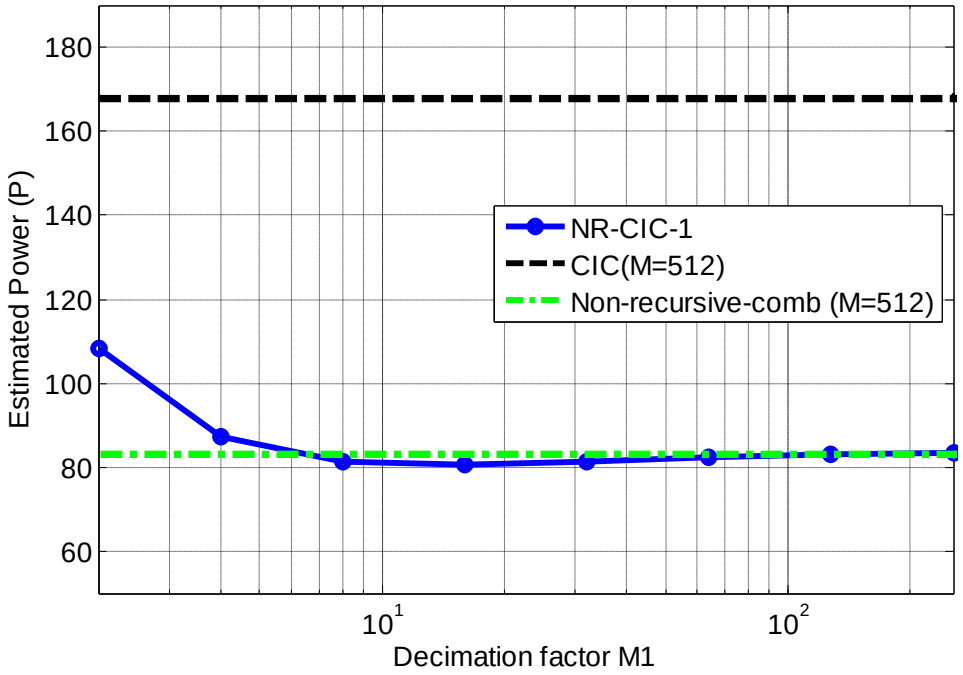
CIC



Non-recursive comb



Stage 0 Stage 8

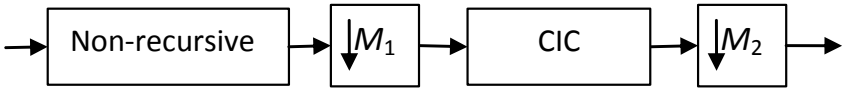


$M_1 \geq 4$

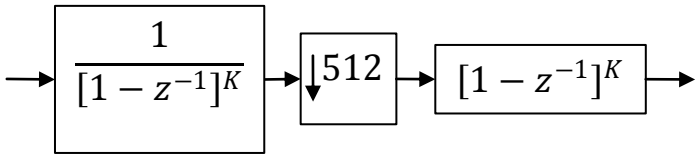
The *NR-CIC-1* structure for $M=2^P$

Example for M=512 (area estimation)

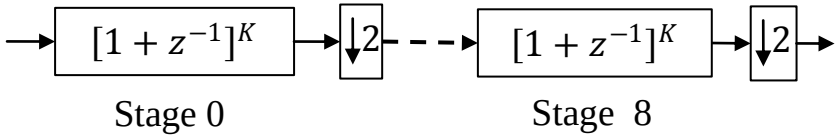
NR-CIC-1 structure

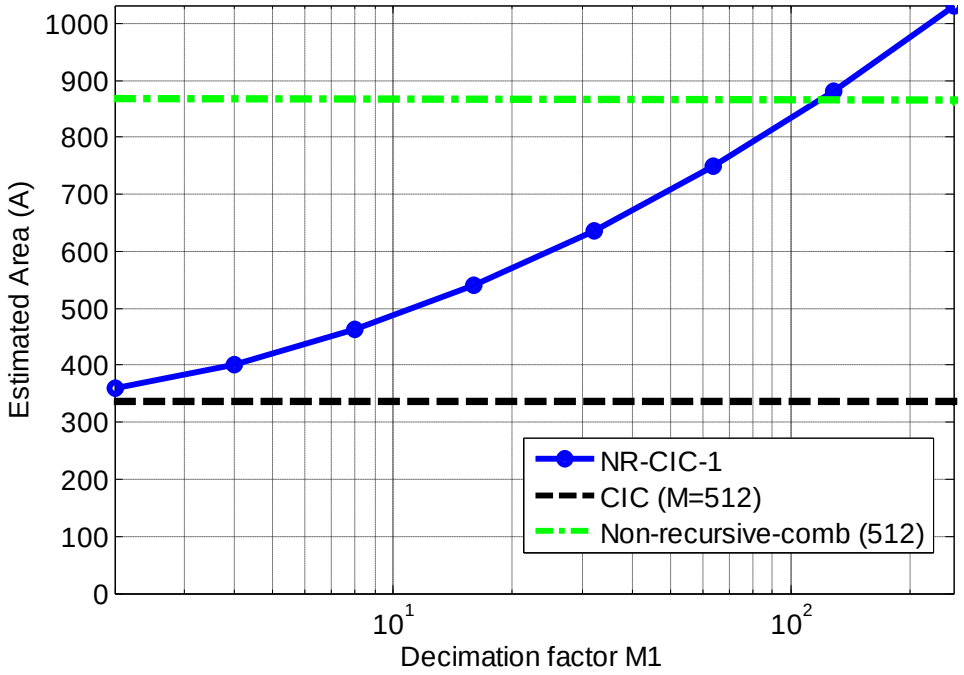


CIC



Non-recursive comb

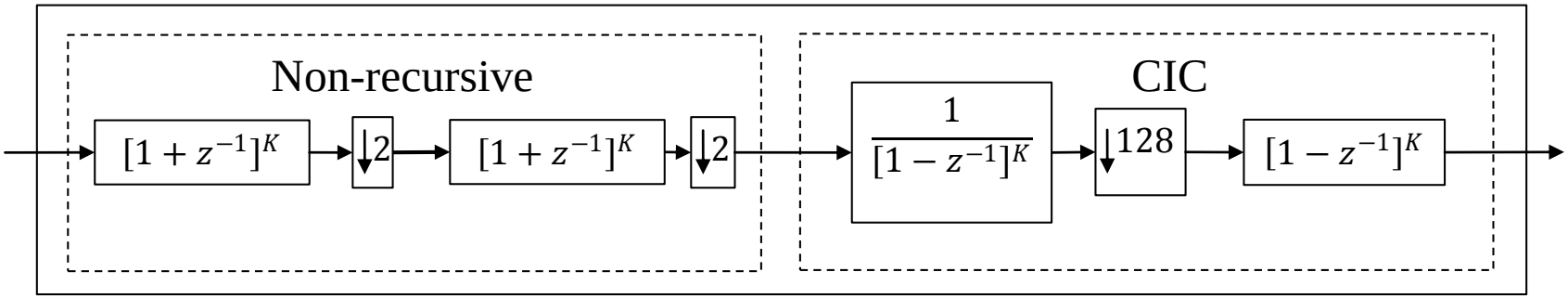




M_1 as low as possible

The *NR-CIC-1* structure for $M=2^P$

Example for M=512 (power estimation)



$M_1=4$ $M_2=128$

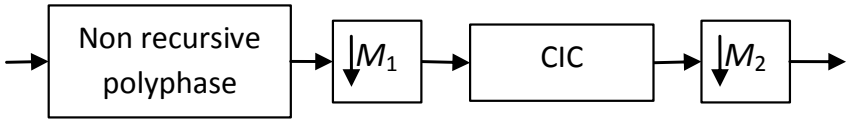
Optimal values for M_1 for different decimation factors

M	M_1
1024	8
2048	
4096	16
8192	

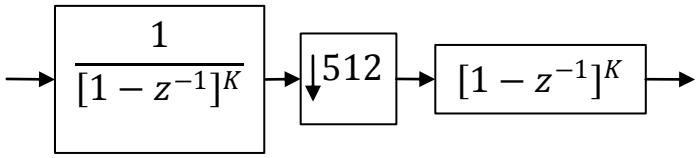
The *NR-CIC-2* structure for $M=2^P$

Example for M=512 (power estimation)

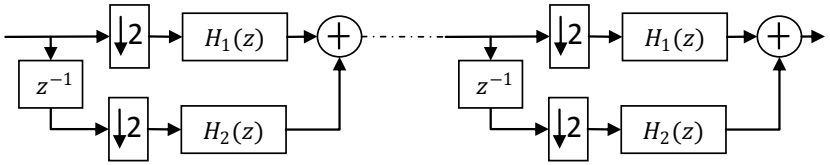
NR-CIC-2 structure

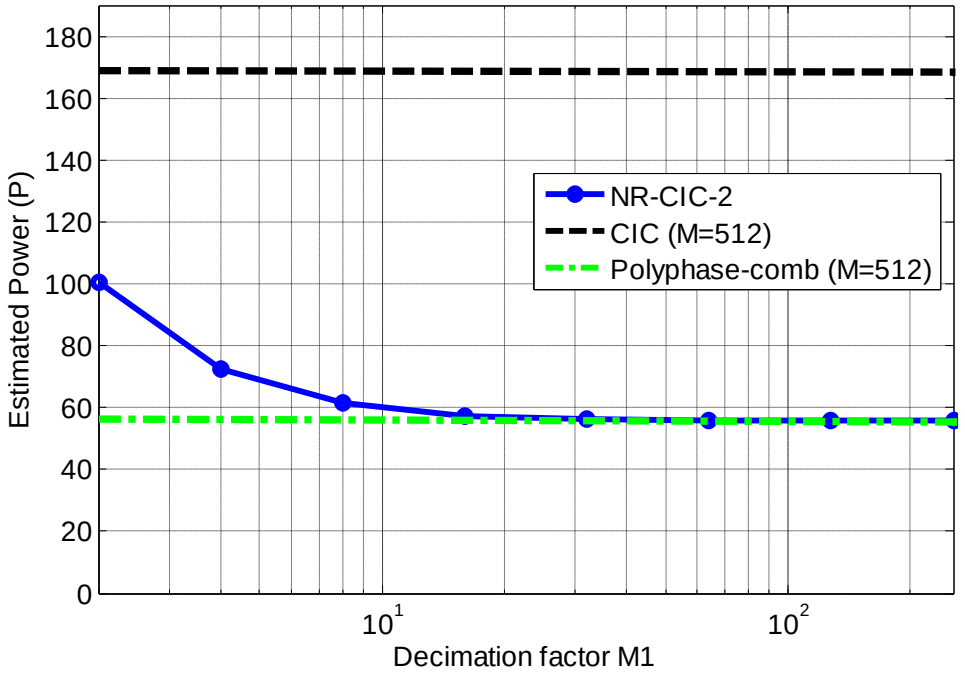


CIC



Non-recursive comb



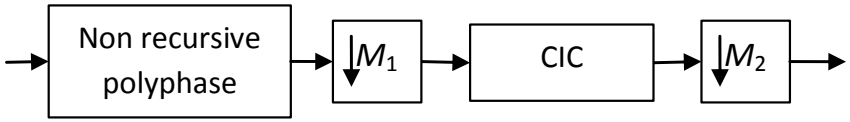


$$M_1 \geq 8$$

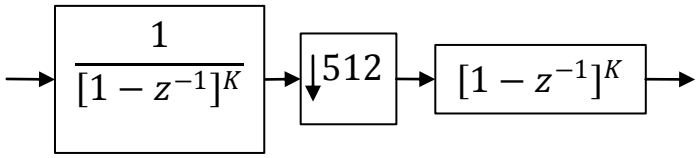
The *NR-CIC-2* structure for $M=2^P$

Example for M=512 (power estimation)

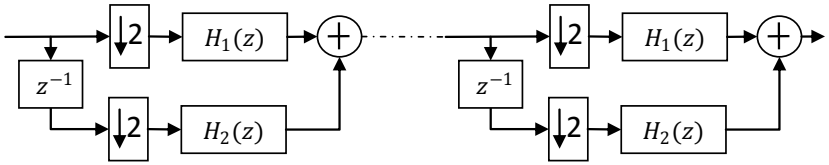
NR-CIC-2 structure

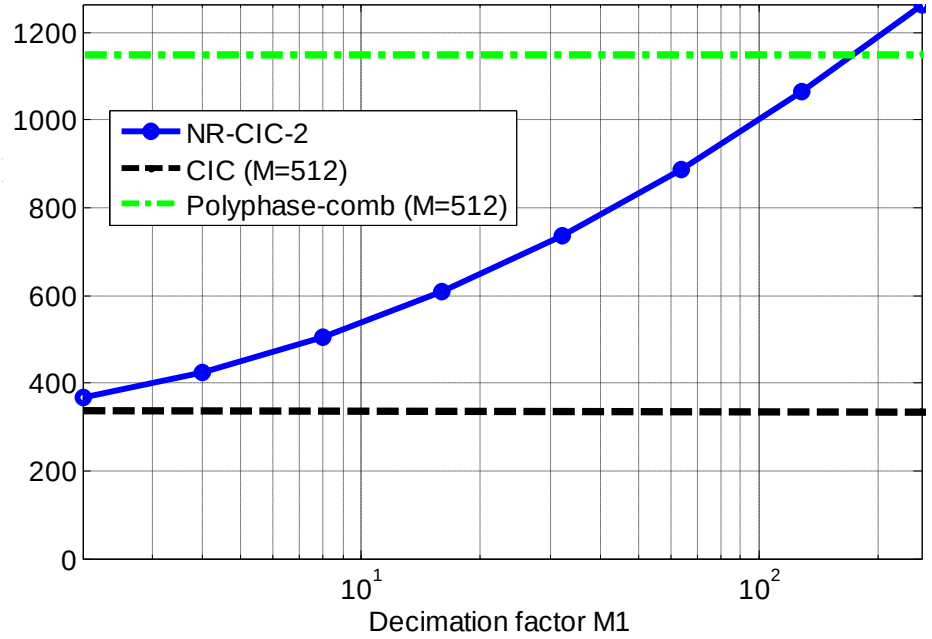


CIC



Non-recursive comb



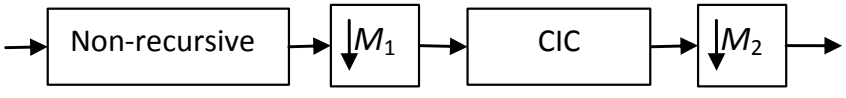


M_1 as low as possible

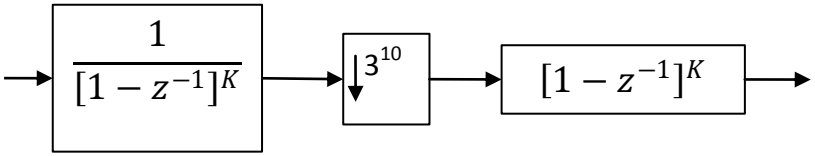
The *NR-CIC-1* structure for $M=3^P$

Example for $M=3^{10}$ (power estimation)

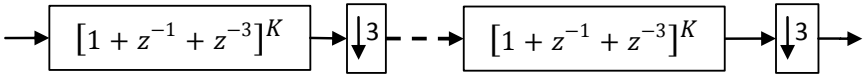
NR-CIC-1 structure



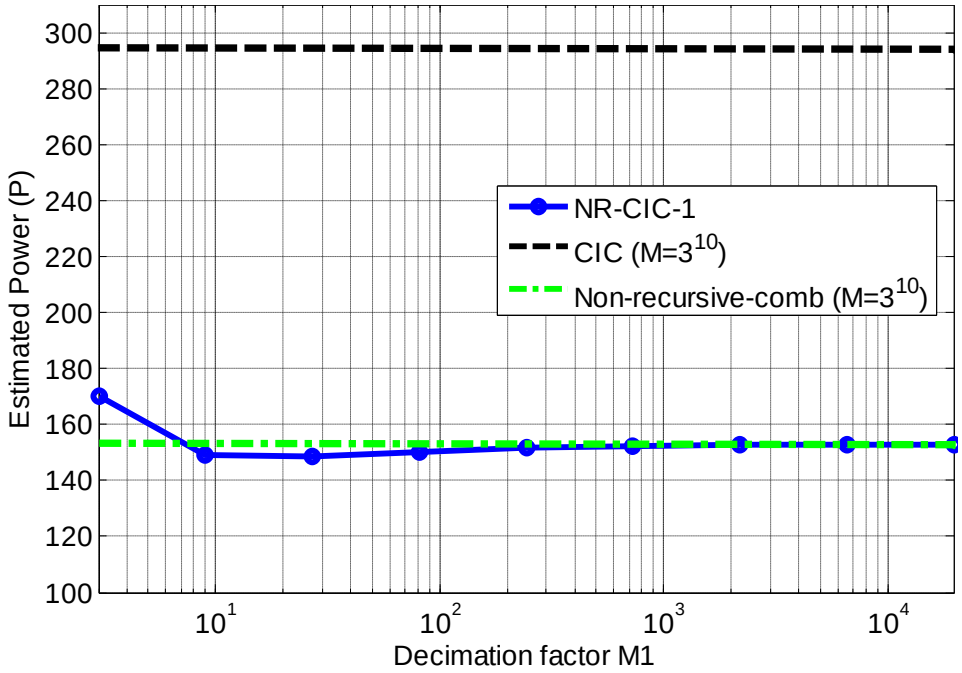
CIC



Non-recursive comb



Stage 0 Stage 9

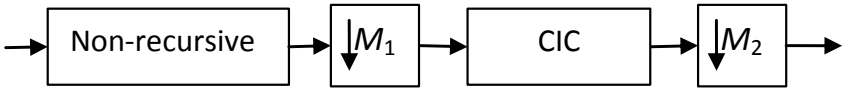


$M_1 \geq 9$

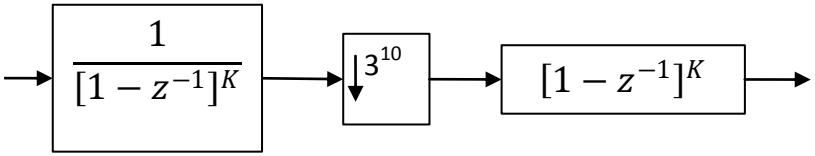
The *NR-CIC-1* structure for $M=3^P$

Example for $M=3^{10}$ (area estimation)

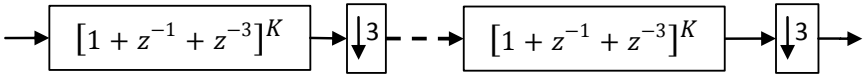
NR-CIC-1 structure



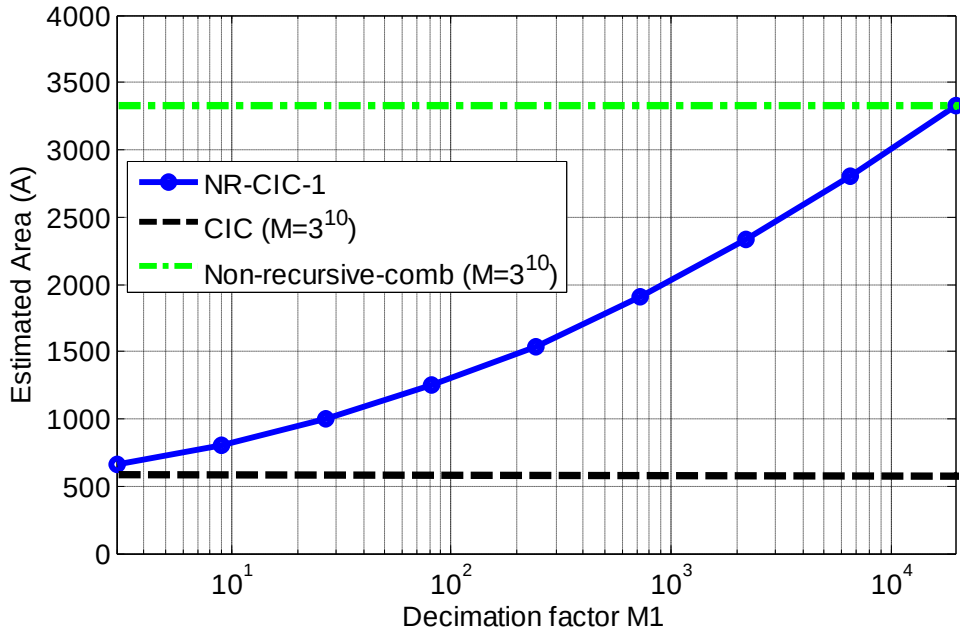
CIC



Non-recursive comb



Stage 0 Stage 9

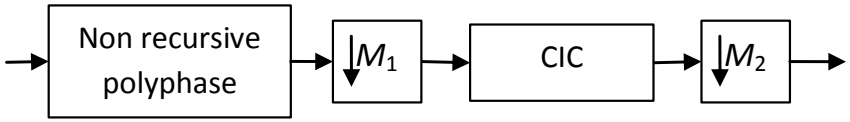


M_1 as low as possible

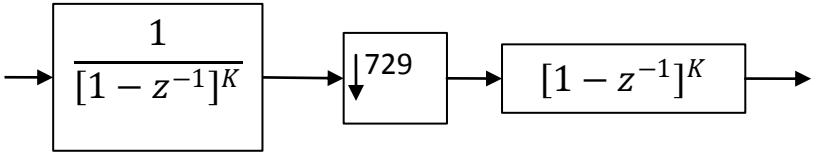
The *NR-CIC-2* structure for $M=3^P$

Example for M=729, power estimation:

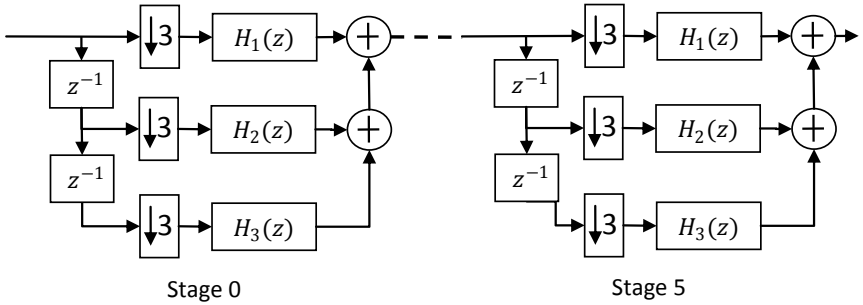
NR-CIC-2 structure

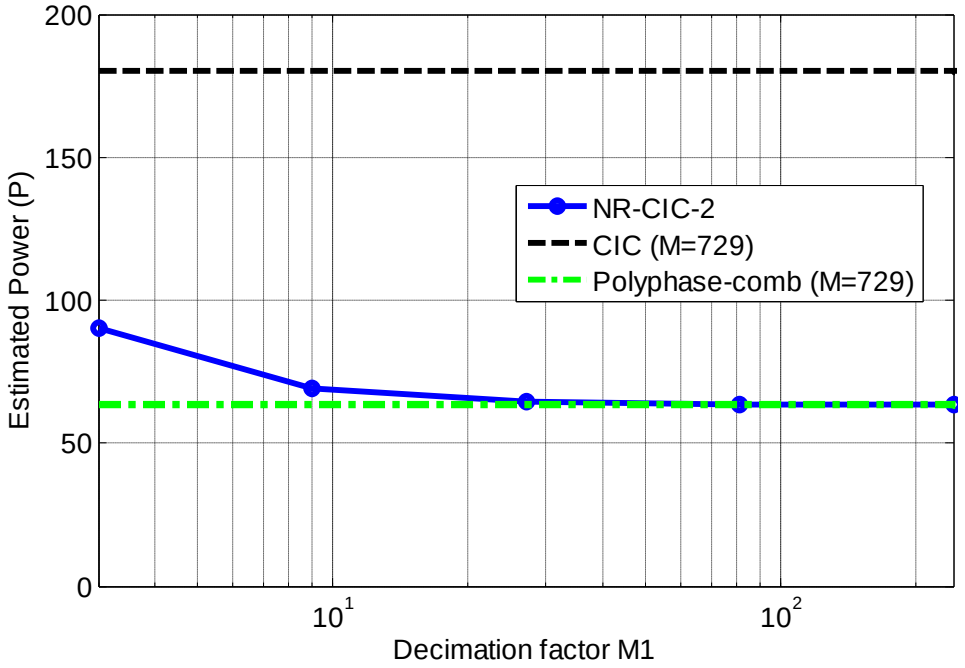


CIC



Polyphase comb



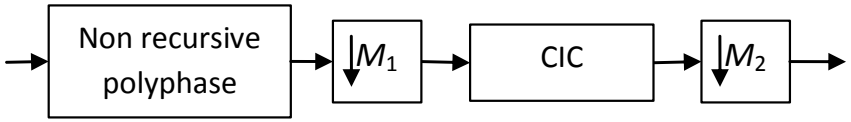


$$M_1 \geq 9$$

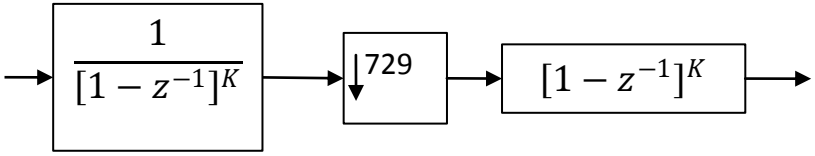
The *NR-CIC-2* structure for $M=3^P$

Example for M=729, power estimation:

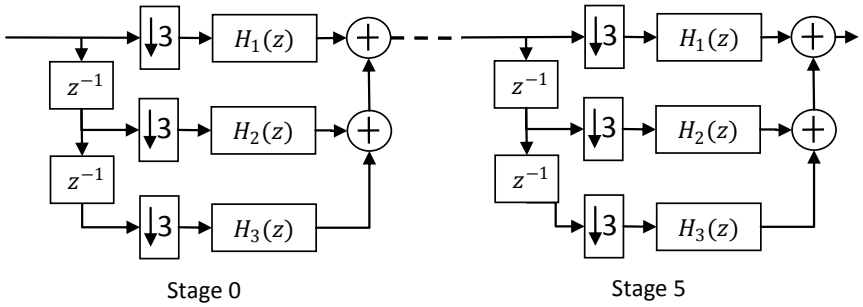
NR-CIC-2 structure

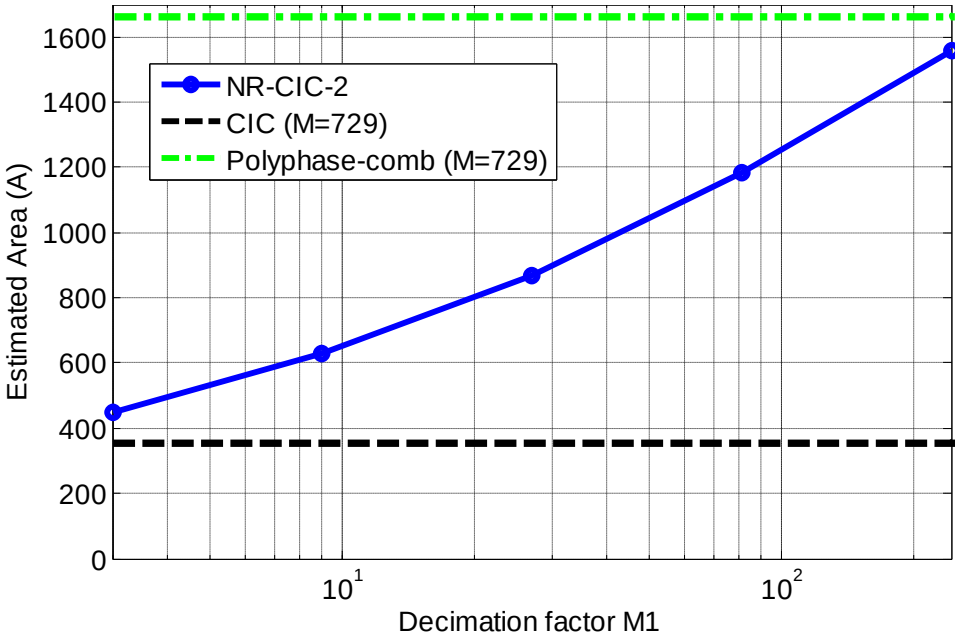


CIC



Polyphase comb





M_1 as low as possible

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Basic NR-comb

$$G(z) = \frac{1}{x}\left(1 + z^{-1} + z^{-2} + z^{-3} \ldots + z^{-(x-1)}\right)$$

Expanded NR-comb by *N*

$$G(z^N) = \frac{1}{x}\left(1 + z^{-N} + z^{-2N} + z^{-3N} \ldots + z^{-(x-1)N}\right)$$

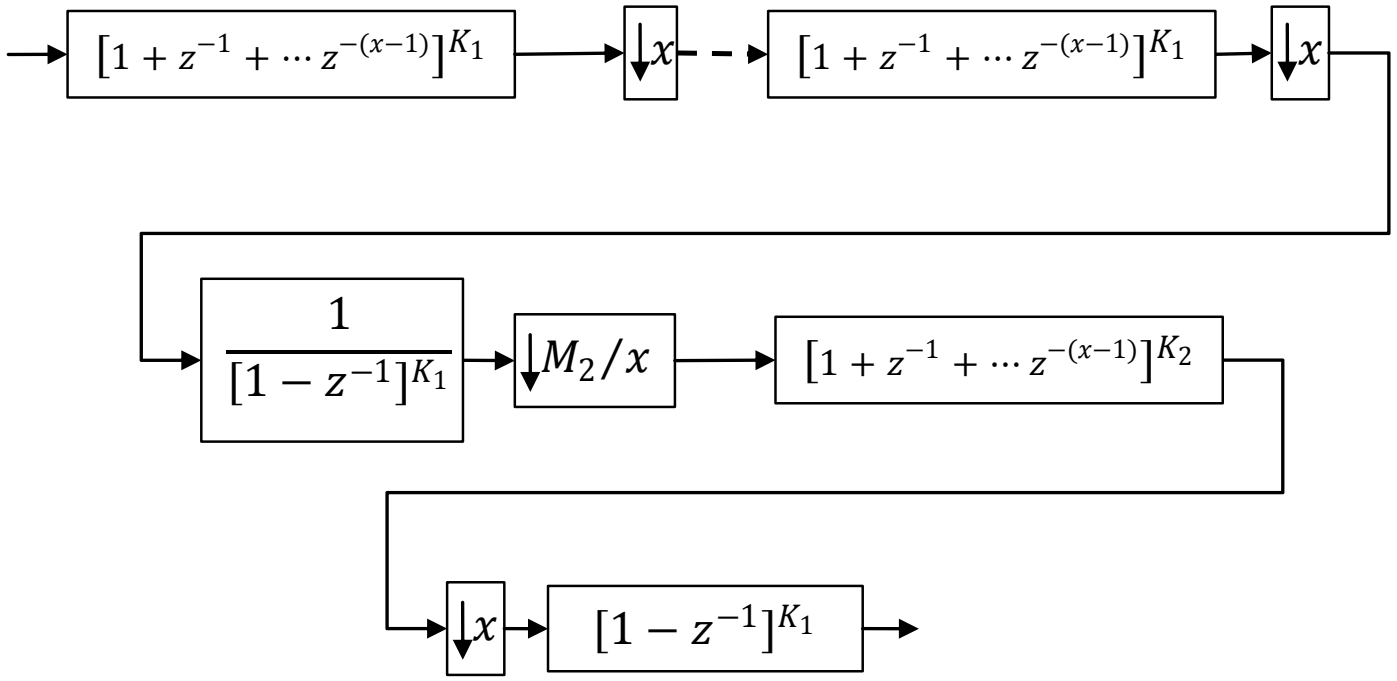
Magnitude response of Expanded NR-comb by *N*

$$\left|G(e^{j\omega N})\right| = \left|\frac{1}{x}\frac{\sin\left(\frac{xN\omega}{2}\right)}{\sin\left(\frac{N\omega}{2}\right)}\right|$$

Zeros at $2\pi/xN$

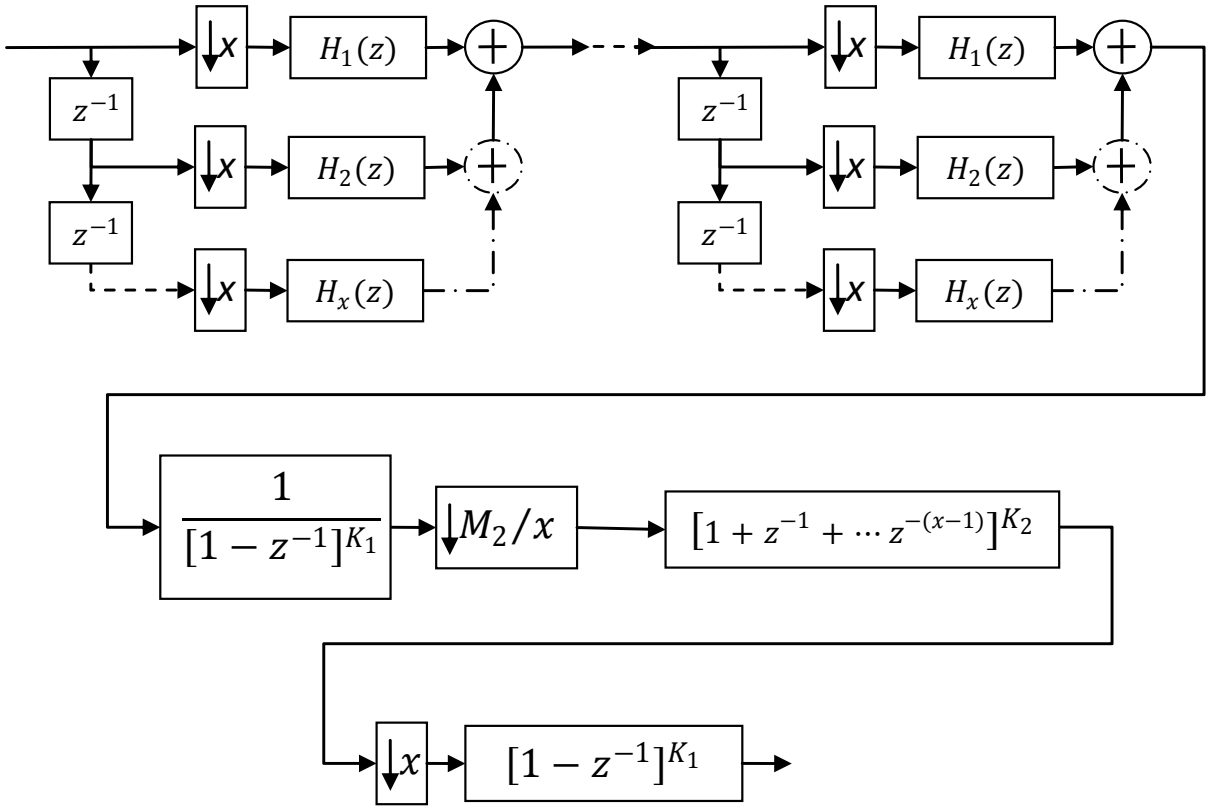
If $N = M/x$, an additional zero is obtained in the first folding band of *NR-CIC*-1,2

NR-Comb-3



K_2 is the cascade of the expanded comb filter.

NR-Comb-4



K_2 is the cascade of the expanded comb filter.

Worst-Case-Attenuation Improvement

$$K_2 = \left\lceil \frac{A_D - A_{NR-CIC-1,2}}{WCAI} \right\rceil$$

WCAI depends on x as follows:

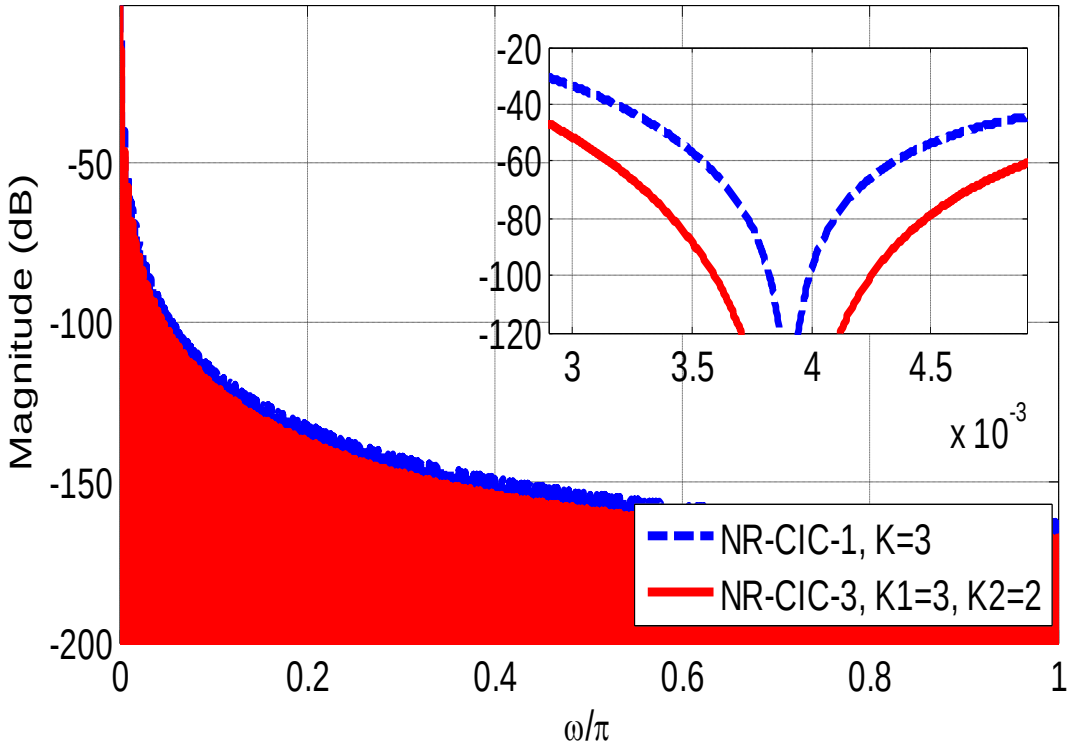
x	WCAI (dB)			
	R=2	R=4	R=8	R=16
2	-8.32	-14.19	-20.17	-26.18
3	-9.54	-15.87	-22.13	-28.29
5	-10.13	-16.68	-23.06	-29.98
7	-10.28	-16.90	-23.31	-29.56
11	-10.38	-17.03	-23.47	-29.73

Example1: *NR-CIC-1* with M_1=4, M_2=128, K=3, and R=2

$$A_{NR-CIC-1} = -30dB$$

$$A_D = -45dB$$

$$K_2 = \left\lceil \frac{|30-45|}{8.34} \right\rceil = \lceil 1.79 \rceil = 2$$

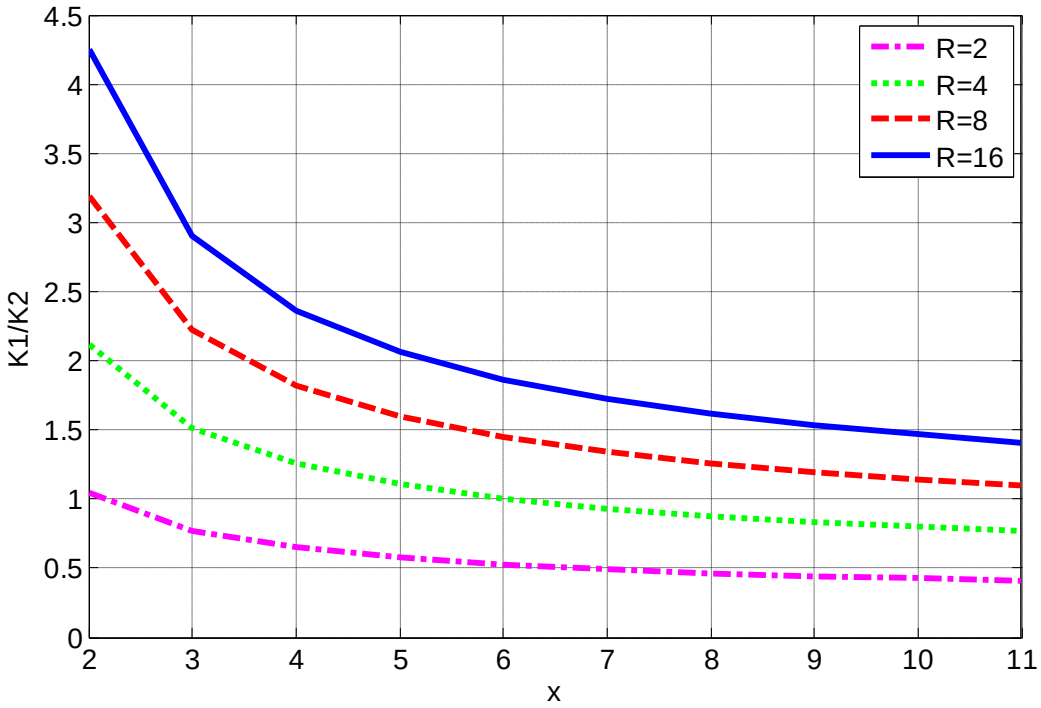


A) Power reduction in NR-CIC-3 and NR-CIC-4

The power of NR-CIC-3 and NR-CIC-4 can be reduced by decreasing K_1.

The WCA reduction should be compensated with K_2, satisfying:

$$\frac{K_1}{K_2} \leq 20log\left\{\frac{\left[\frac{1}{x}\frac{\sin\left(\frac{\pi(2xR-1)}{2R}\right)}{\sin\left(\frac{\pi(2xR-1)}{2xR}\right)}\right]}{\left[\frac{1}{x}\frac{\sin\left(\frac{\pi(2R-1)}{2R}\right)}{\sin\left(\frac{\pi(2R-1)}{2xR}\right)}\right]} - \frac{\left[\frac{\sin\left(\frac{\pi(2R-1)}{2R}\right)}{\left(\frac{\pi(2R-1)}{2R}\right)}\right]}{\left[\frac{\sin\left(\frac{\pi(2xR-1)}{2R}\right)}{\left(\frac{\pi(2xR-1)}{2R}\right)}\right]}\right\}$$

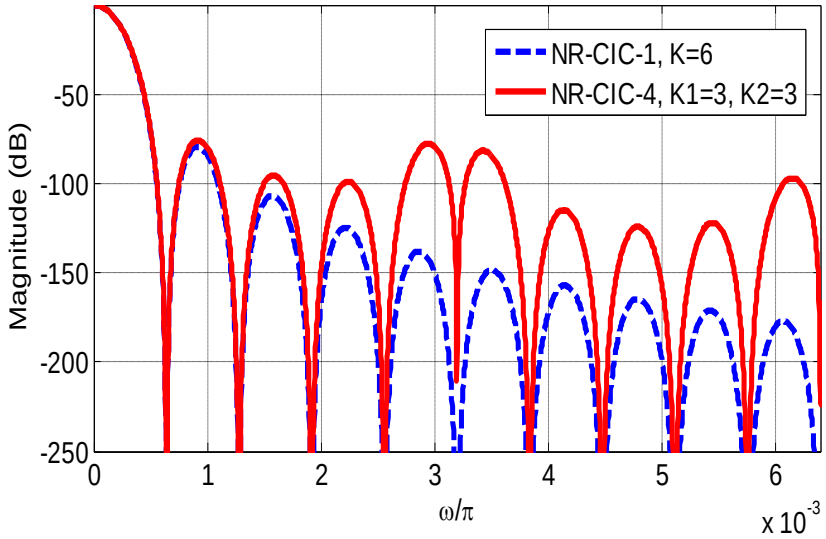


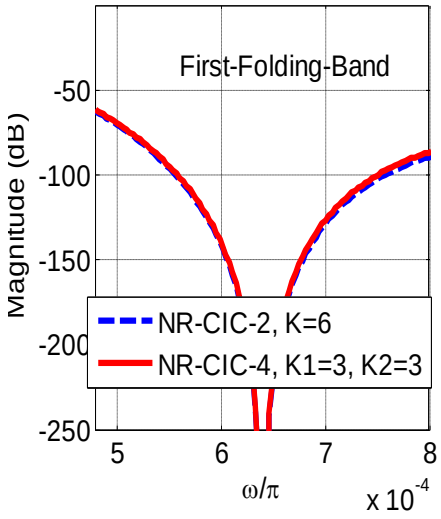
A) Power reduction in NR-CIC-3 and NR-CIC-4

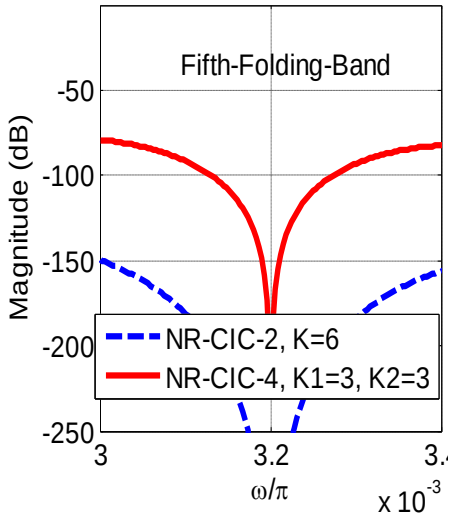
Example 2:

NR-CIC-2 with M_1=5, M_2=625, R=2 and K=6 has a WCA = -60dB.

NR-CIC- 4 with K_1=3 and K_2=3 also has a WCA = -60dB ($K_1/K_2 \leq 1.1$)







K_1 from 6 to 3 leads to a power savings of around 45%.

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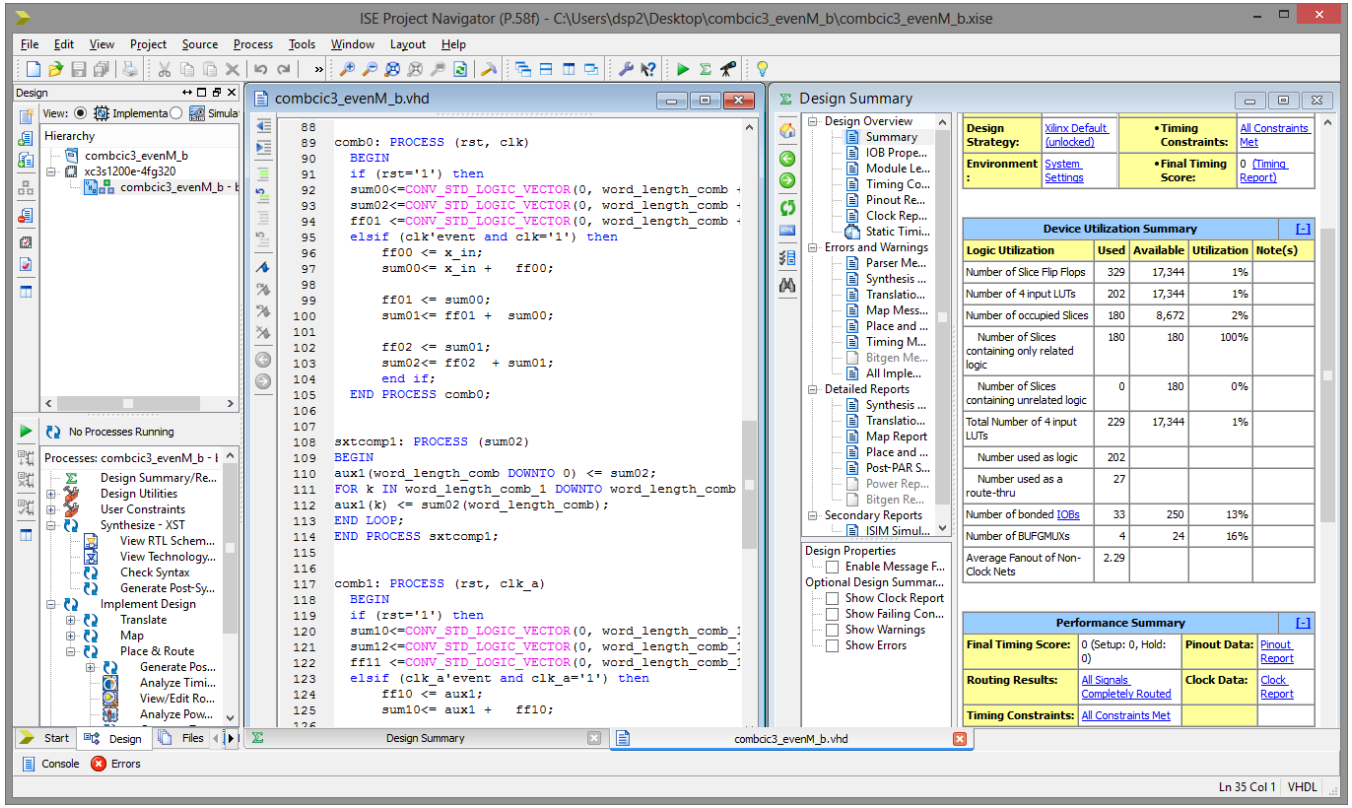
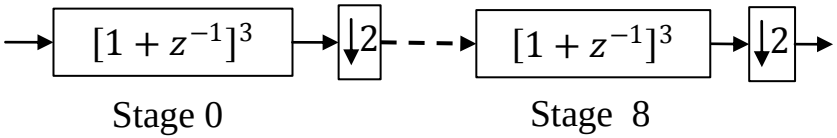
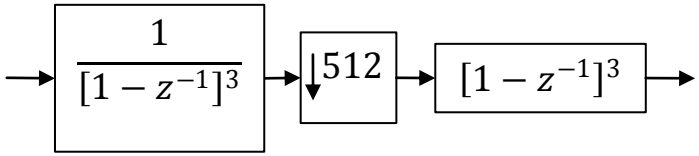
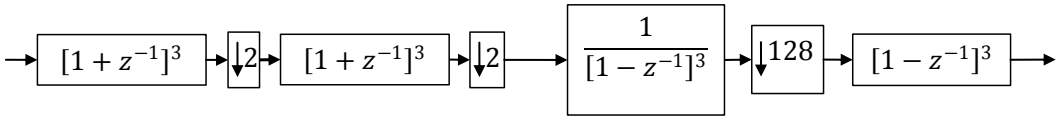
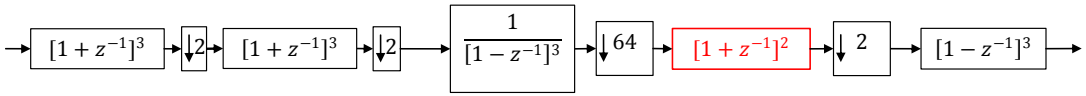
Decimators are implemented at the RTL in the VHDL



- A 0.18μm CMOS process is considered.
- Power is estimated at the transistor-level and area is taken from the layouts.
- One-bit ΣΔ modulator is considered as the input for decimators.

Power and area implementation results for the Example 1

PS=1.8V, F_{in}= 10MHz, M=512, F_{out}= 19.5kHz.

	Power (μW)	Area (μm²)	WCA (dB)
Non-recursive comb  	**226**	**424,569**	30
CIC  	**408**	**326,041**	30
Two-Stage Structure  	**235**	**339,309**	30
Improved Two-Stage Structure  	**238**	**423,832**	**46**

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- Several novel two-stage efficient comb-based decimation structures for high values of the decimation factors, which are power of any prime number *x*, have been presented.

- *NR-CIC*-1 and *NR-CIC*-2 structures take the power benefits of non-recursive-comb and the area efficiency of CIC structure.

- The choice of the decimation factors M_1 and M_2, which makes the best balance of area and power efficiency, is elaborated.

- The presented modified structures *NR-CIC*-3 and *NR-CIC*-4 have improved alias rejections in the first folding band, and in all other folding bands which are not factors of *x*.

- The efficiency of the proposed structures has been validated considering a 0.18μm CMOS technology, taking x=2 and M=512 as an example.

- The obtained results confirm that the proposed structures are efficient solutions for the implementation of ΣΔ ADCs converters with high values of the oversampling ratio.

- The compensation of the passband droop has not been considered, because the problem can be solved by cascading any simple known *multiplierless* compensator at lower rate.


Thank you!